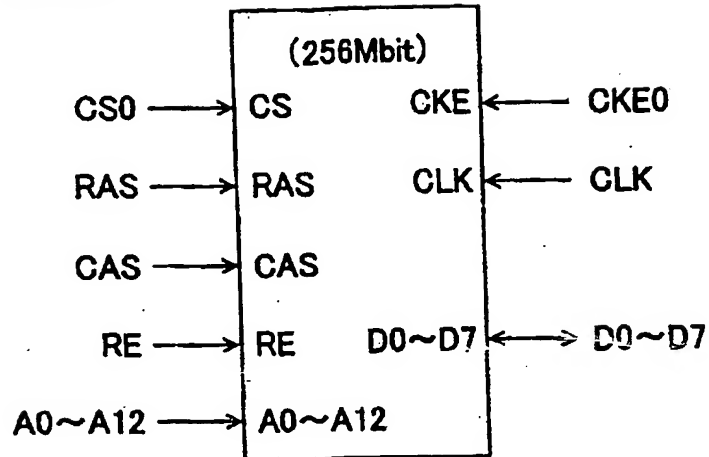


FIG. 1



FIG. 2

BANK1



BANK2

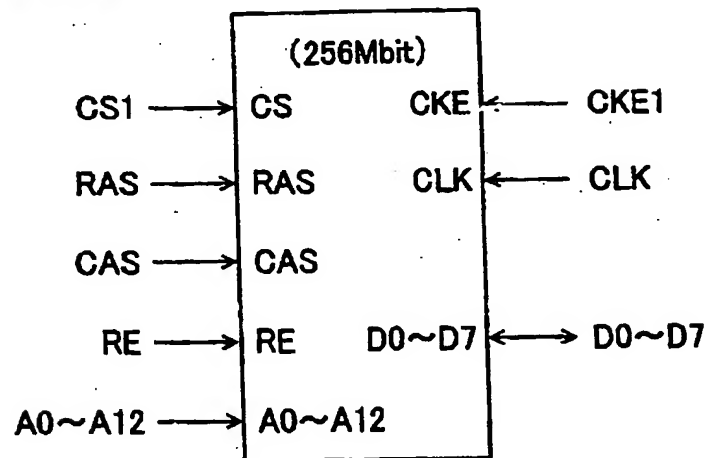
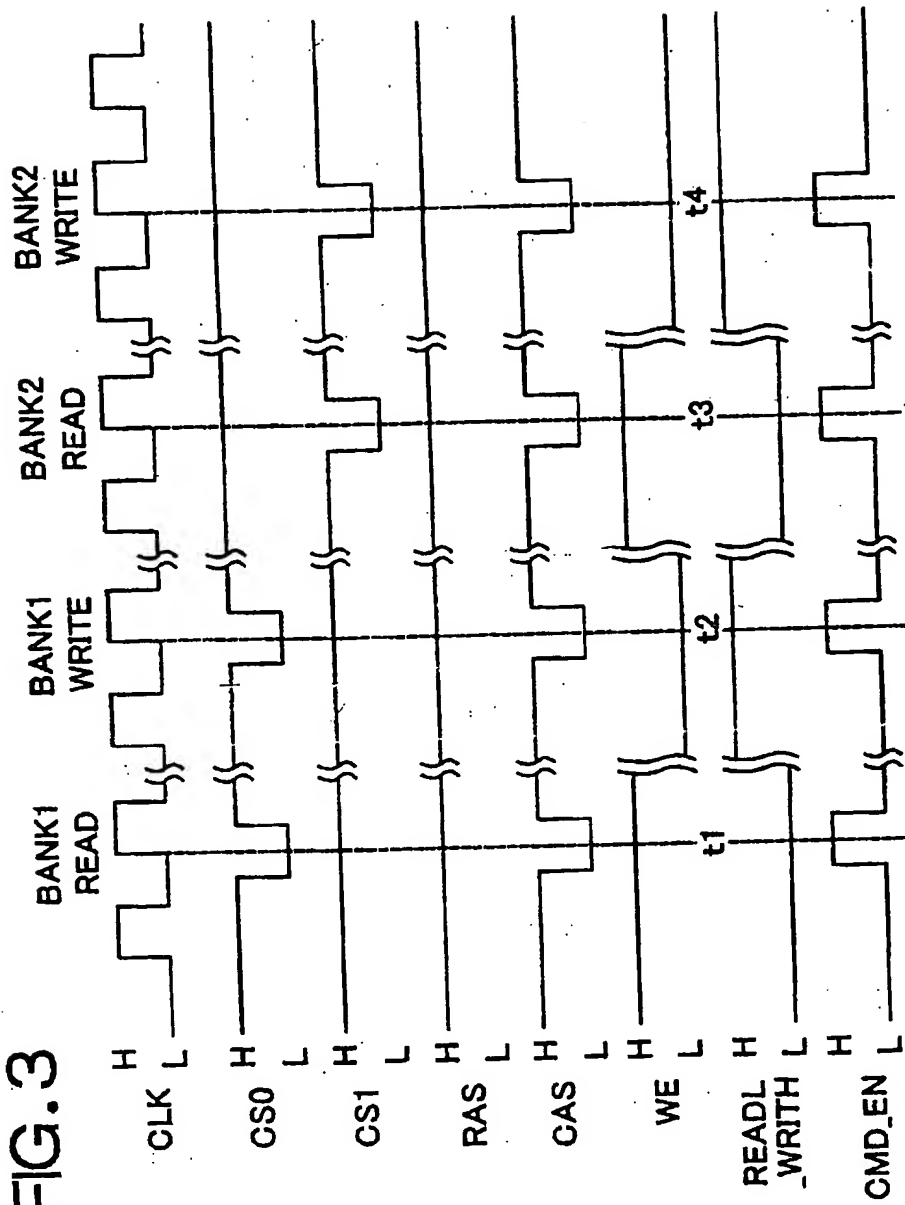




FIG. 3



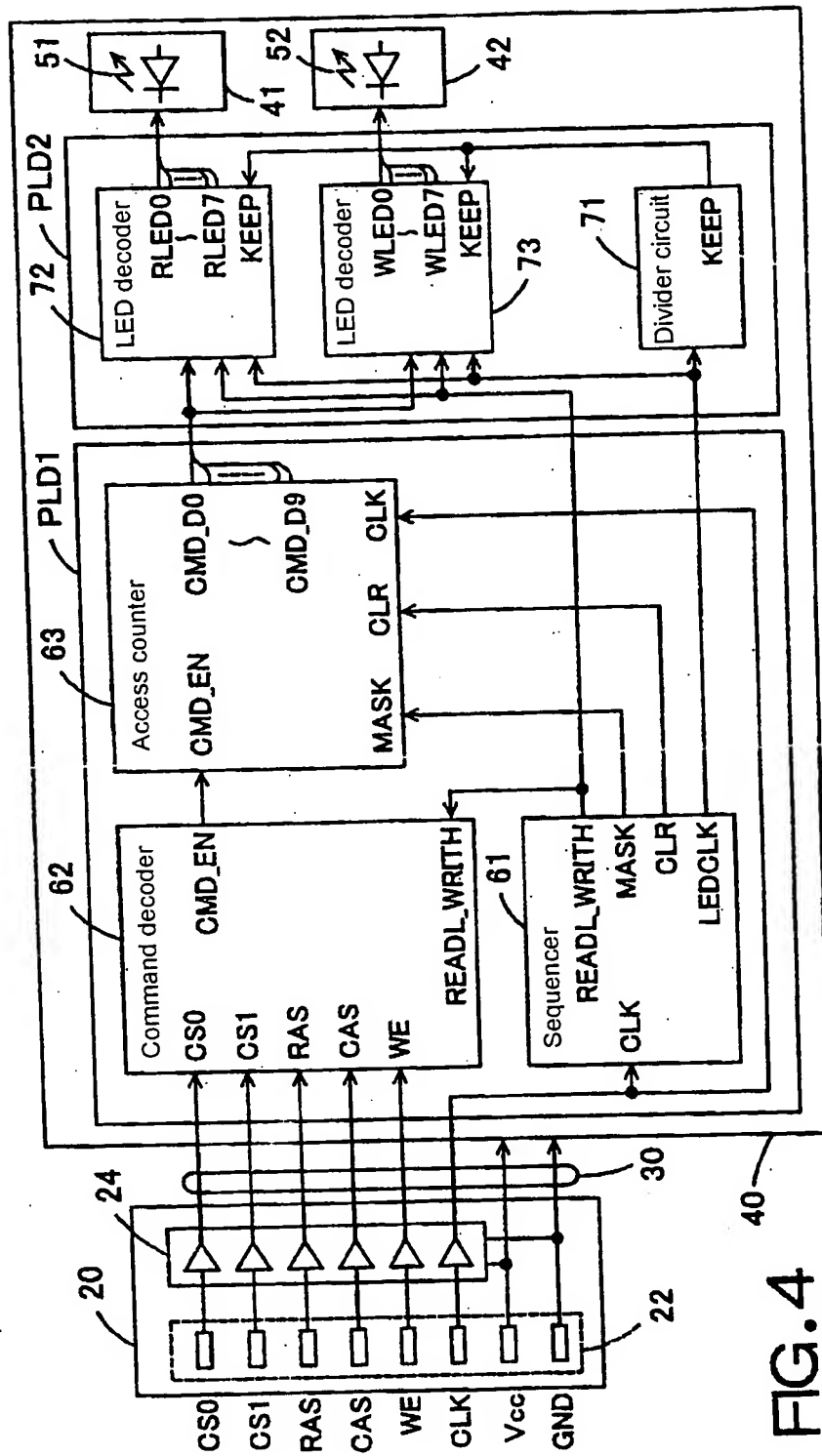


FIG. 4



FIG. 5

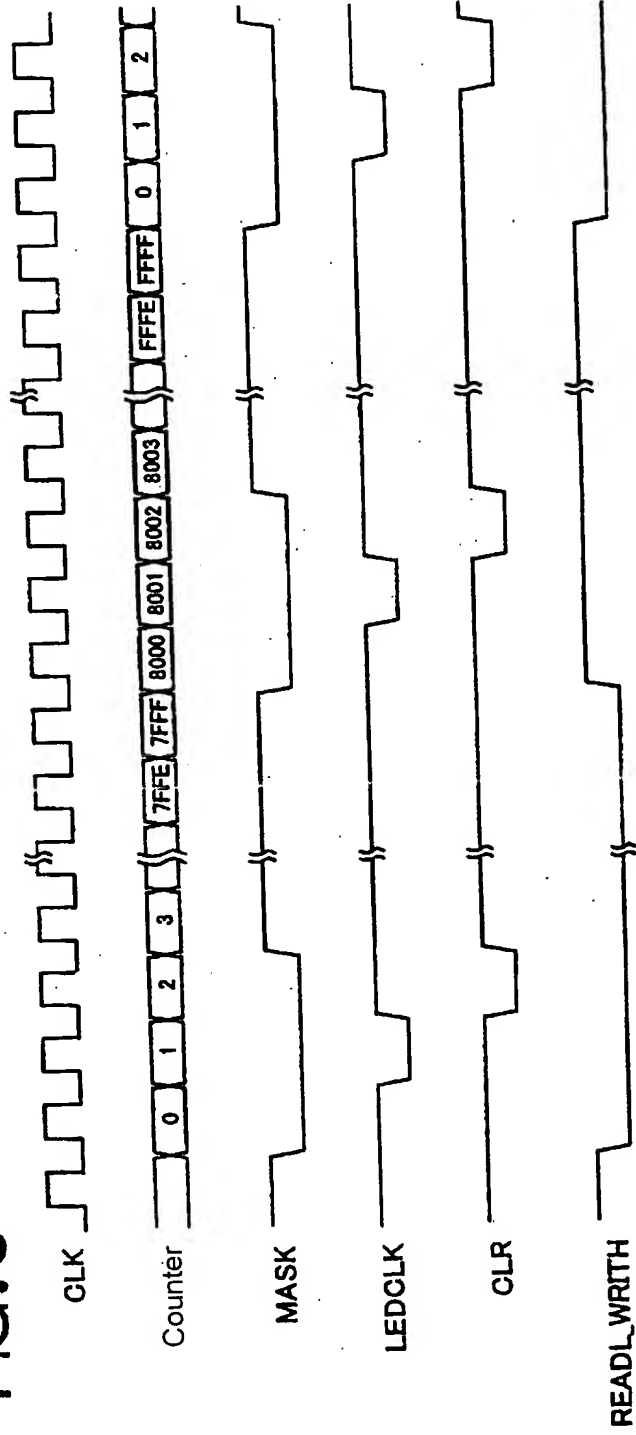




FIG. 6

T1

Counter	Output
0 0 0 0	MASK → L
0 0 0 0	LEDCLK → H
0 0 0 0	CLR → H
0 0 0 0	READL_WRITH → L
0 0 0 1	LEDCLK → L
0 0 0 2	LEDCLK → H
0 0 0 2	CLR → L
0 0 0 3	CLR → H
0 0 0 3	MASK → H
8 0 0 0	MASK → L
8 0 0 0	READL_WRITH → H
8 0 0 1	LEDCLK → L
8 0 0 2	LEDCLK → H
8 0 0 2	CLR → L
8 0 0 3	CLR → H
8 0 0 3	MASK → H

FIG. 7

Command decoder 62

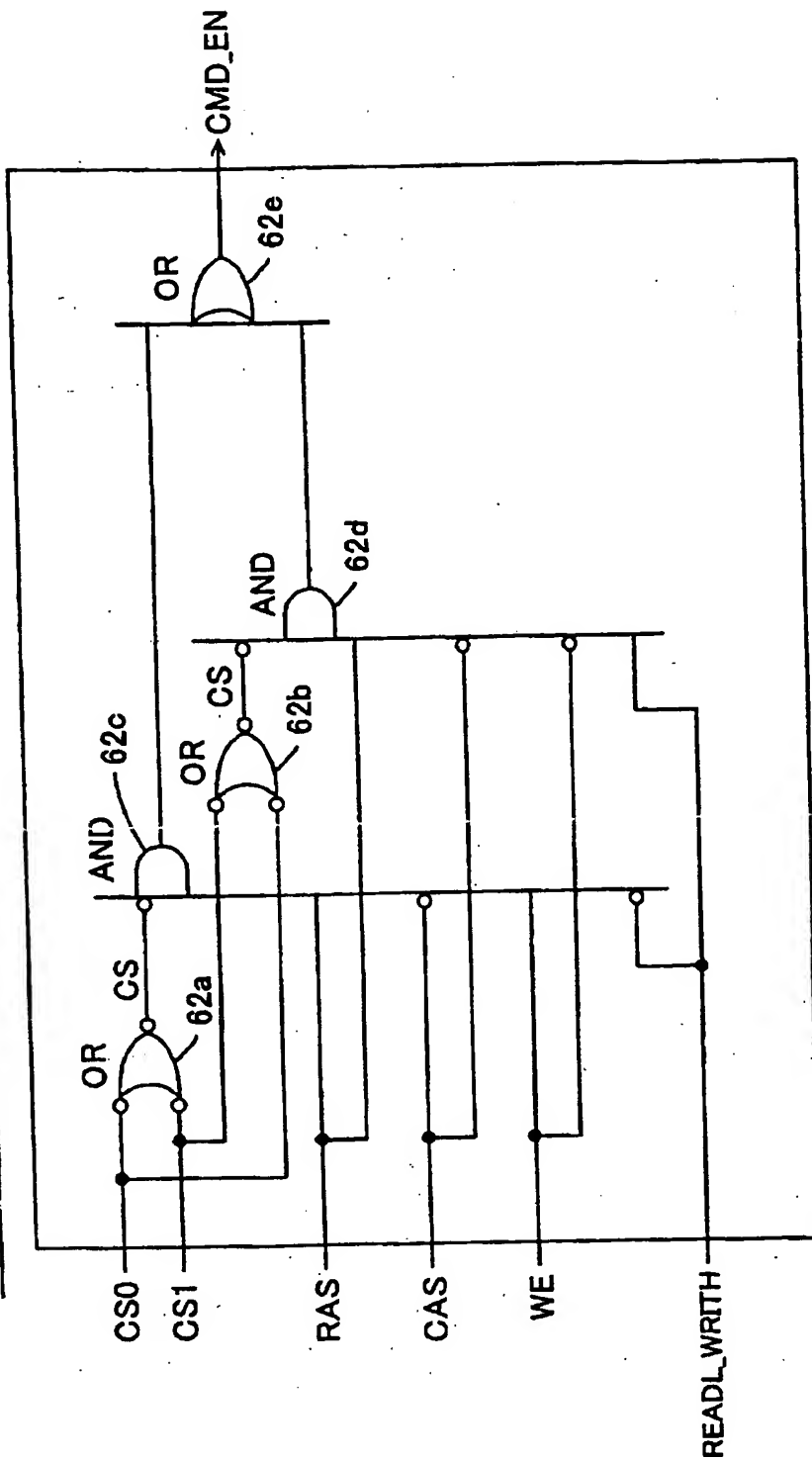




FIG. 8

FUNCTION TABLE

Input					Output
CS	RAS	CAS	WE	READL_WRITH	CMD_EN
H	X	X	X	X	L
L	L	X	X	X	L
L	X	H	X	X	L
L	H	L	H	H	L
L	H	L	H	L	H
L	H	L	L	H	H
L	H	L	L	L	L



FIG. 9

Access counter **63**

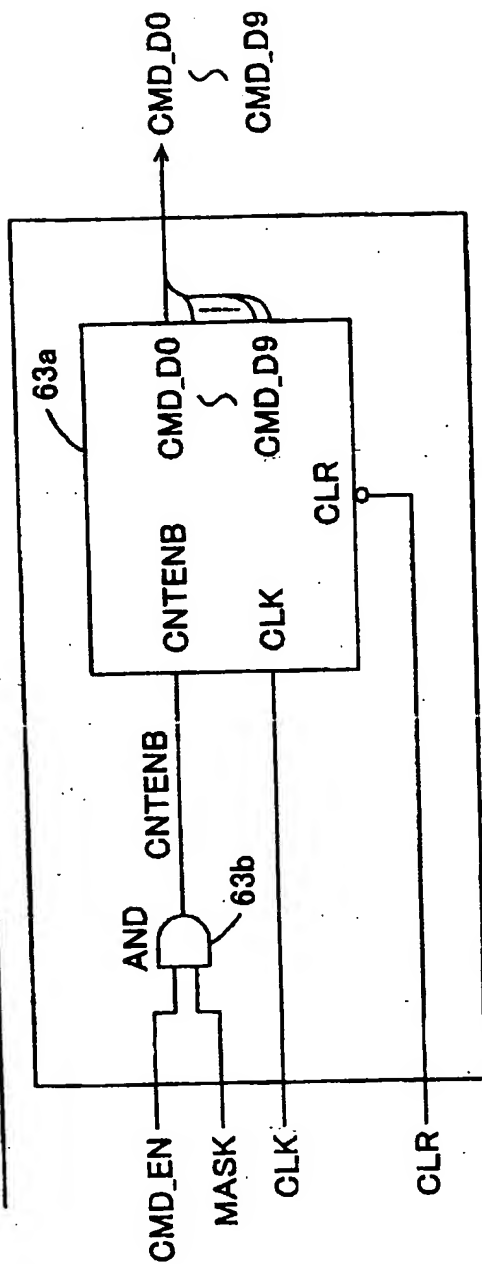




FIG. 10

FUNCTION TABLE

Input				Output
CMD_EN	MASK	CLR	CLK	CMD_D
X	X	L	X	All bit "0"
L	L	H	X	} Stop count
H	L	H	X	
L	H	H	X	
H	H	H	↗	Increment count 0000000000 ← 0000000001 ↓ 1111111110 1111111111 →



FIG. 11

Divider circuit 71

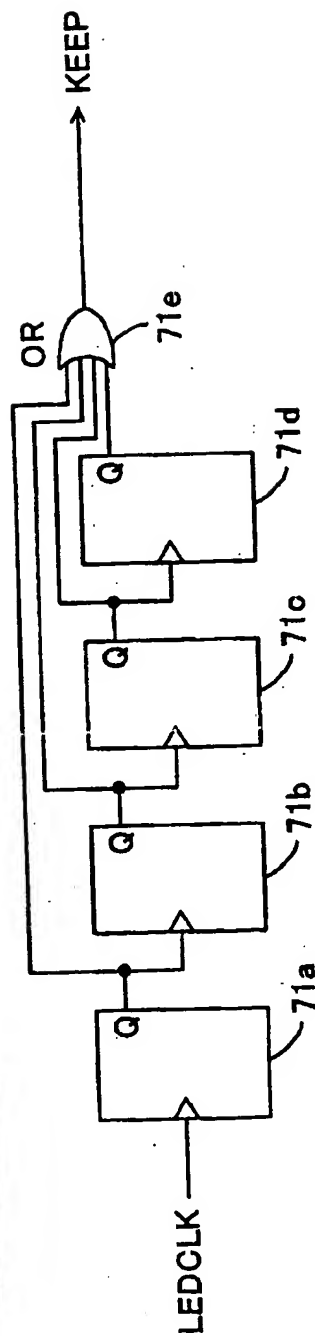
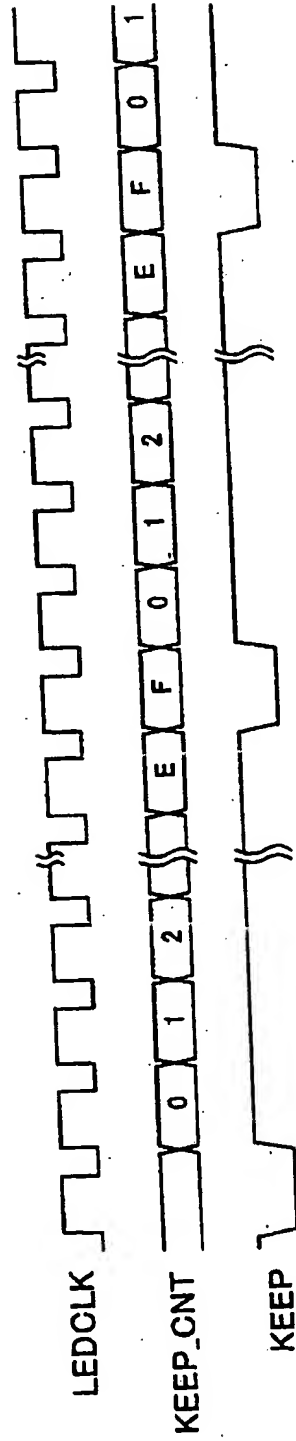




FIG. 12



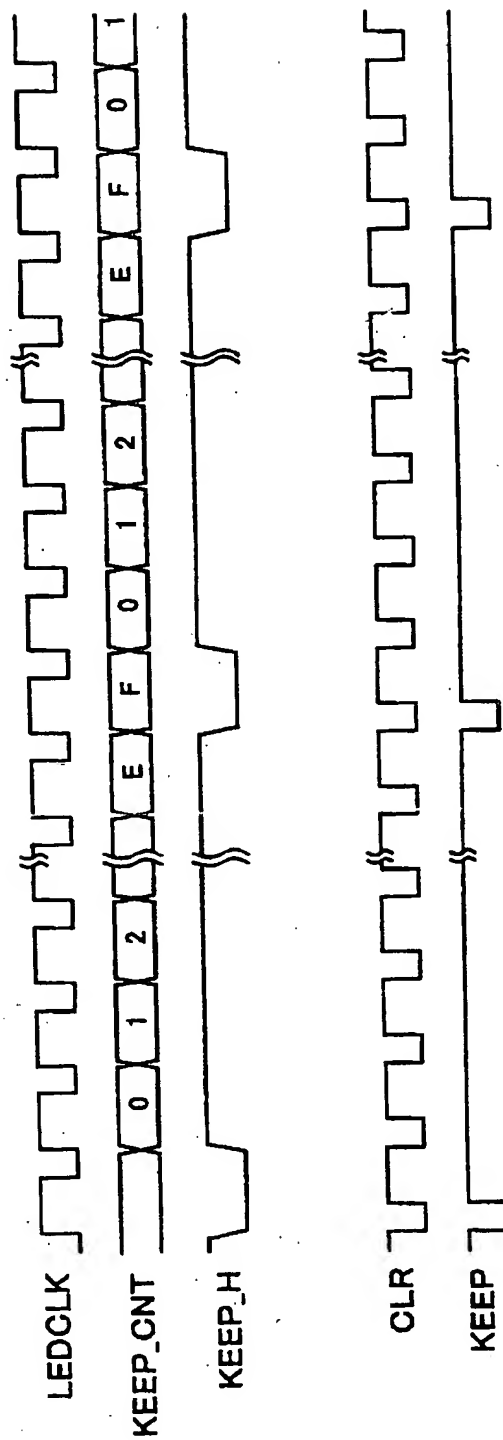
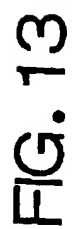


FIG. 14

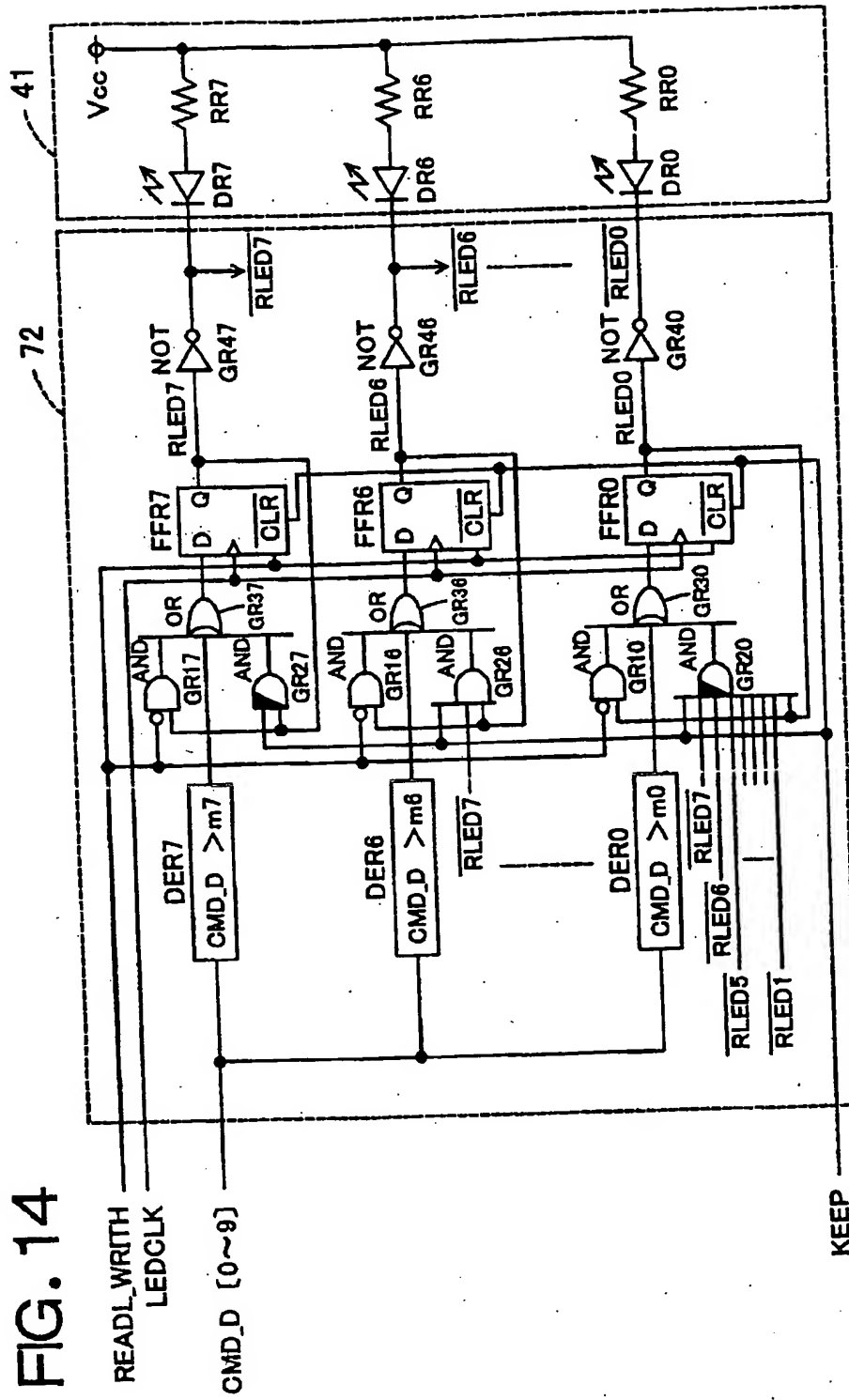


FIG. 15

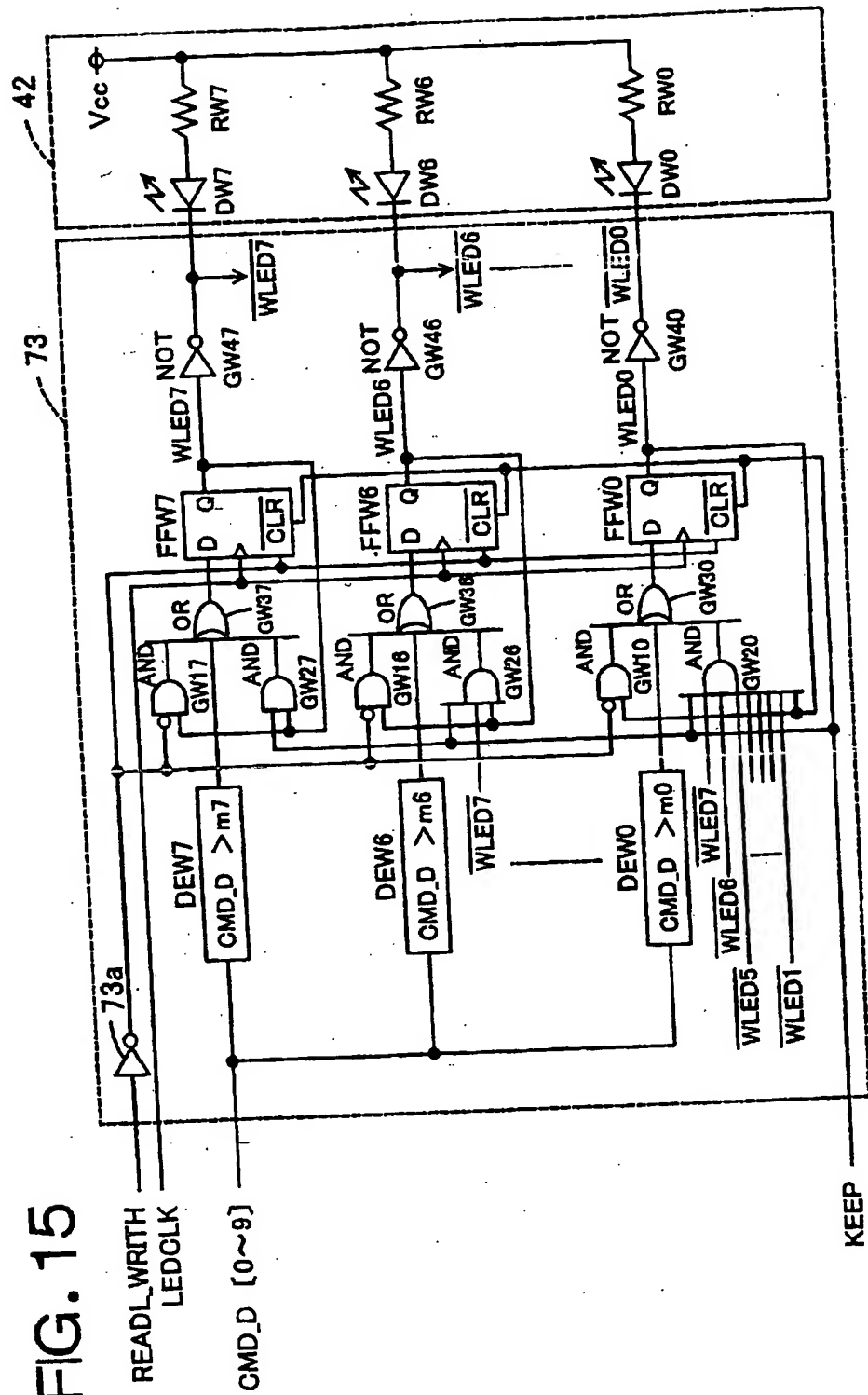




FIG. 16

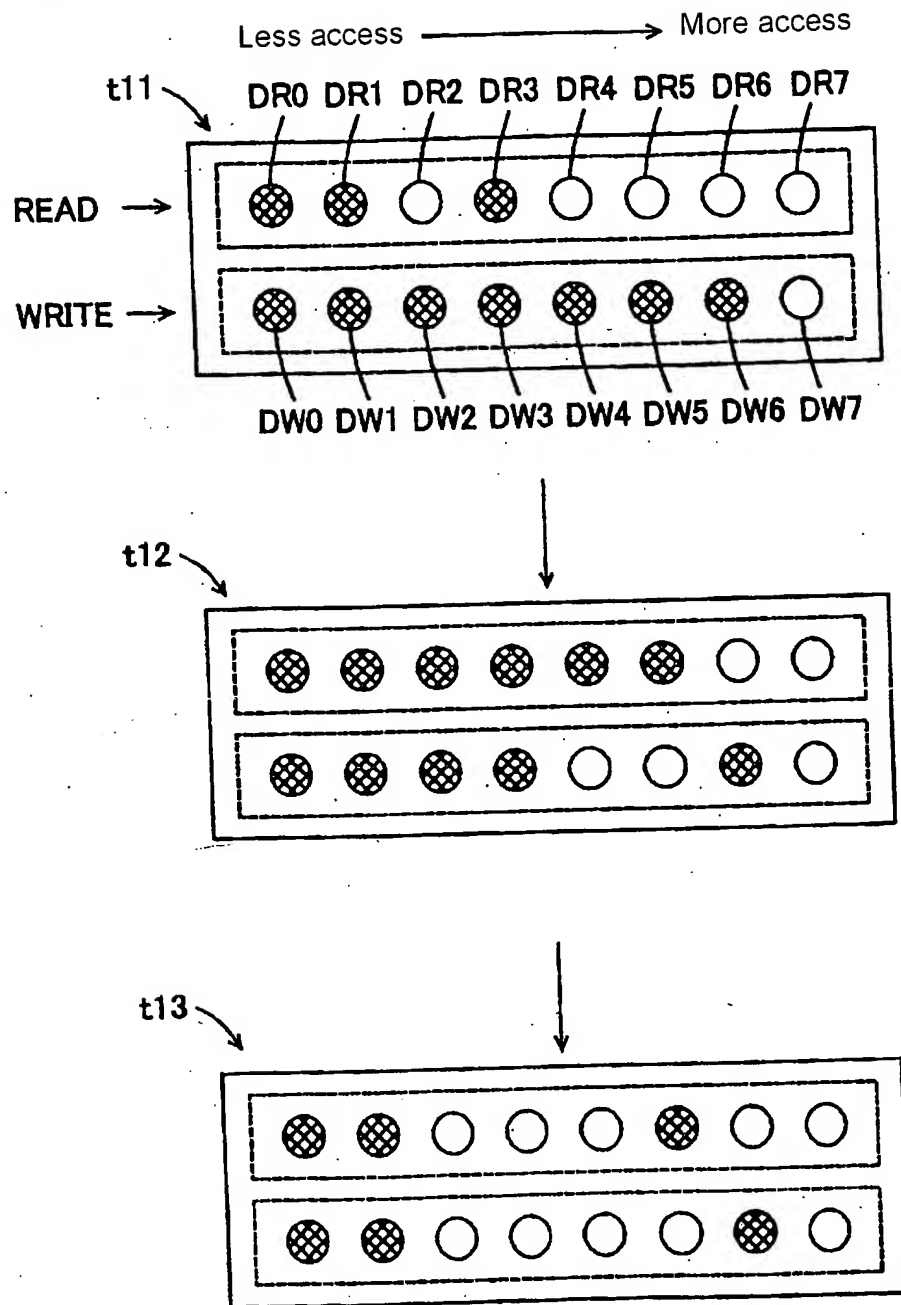




FIG. 17

FUNCTION TABLE

Input	Output							
	DER0	DER1	DER2	DER3	DER4	DER5	DER6	DER7
CMD_D	L	L	L	L	L	L	L	L
CMD_D ≤ m0	H	L	L	L	L	L	L	L
m0 < CMD_D ≤ m1	H	H	L	L	L	L	L	L
m1 < CMD_D ≤ m2	H	H	H	L	L	L	L	L
m2 < CMD_D ≤ m3	H	H	H	H	L	L	L	L
m3 < CMD_D ≤ m4	H	H	H	H	H	L	L	L
m4 < CMD_D ≤ m5	H	H	H	H	H	H	L	L
m5 < CMD_D ≤ m6	H	H	H	H	H	H	H	L
m6 < CMD_D ≤ m7	H	H	H	H	H	H	H	H
m7 < CMD_D	H	H	H	H	H	H	H	H



FIG. 18

FUNCTION TABLE

Input						Output
READL _WRITH	DERi	RLEDi	KEEP	$\overline{\text{RLEDj}}$	LEDCLK	RLEDi
X	X	X	L	X	X	L
L	X	X	H	X	X	RLEDi
H	L	L	H	X	\downarrow	L
H	H	X	H	X	\downarrow	H
H	L	H	H	ALL H	\downarrow	H
H	L	H	H	(L)	\downarrow	L

j=i+1~7



FIG. 19

FUNCTION TABLE

Input						Output
READL _WRITH	DEWi	WLEDi	KEEP	WLEDj	LEDCLK	WLEDi
X	X	X	L	X	X	L
H	X	X	H	X	X	WLEDi
L	L	L	H	X		L
L	H	X	H	X		H
L	L	H	H	ALLH		H
L	L	H	H	(L)		L

j=i+1~7

